SOLID-STATE IMAGING DEVICE AND METHOD FOR DRIVING THE SAME

This non-provisional application claims priority under 35 U.S.C., §119(a), on Patent Application No. 2003-032847 filed in Japan on February 10, 2003, the entire contents of which are hereby incorporated by reference.

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION:

The present invention relates to a solid-state imaging device, for example, a threshold voltage modulation system MOS image sensor, and a method for driving the same.

2. DESCRIPTION OF THE RELATED ART:

An amplification type solid-state imaging device is nowadays widely used as a solid-state imaging device, in which each of unit pixels has a signal amplification function and signals are sequentially read from each unit pixel by a scanning circuit. Such an amplification type solid-state imaging device is available in a planar type and a vertical type. In a planar type amplification type solid-state imaging device, elements including a reset section and a pixel selection section are arranged in a

planar manner in each unit pixel. In a vertical type amplification type solid-state imaging device, such elements are arranged vertically.

For example, Japanese Laid-Open Publications Nos. 11-195778 and 2002-134729 propose a vertical type amplification type solid-state imaging device which is called a threshold voltage modulation system MOS image sensor. This image sensor includes a MOS transistor (insulation gate type field effect transistor) for detecting a signal corresponding to an amount of light and a carrier pocket (charge accumulation region) provided below a channel region of the MOS transistor.

A threshold voltage modulation system MOS image sensor (also referred to simply as "MOS image sensor" or "image sensor") will be described in detail with reference to Figures **6A** and **6B**.

Figures **6A** and **6B** show a part of the threshold voltage modulation system MOS image sensor. Figure **6A** is a top view of a unit pixel section **10**, which corresponds to one pixel of the image sensor. Figure **6B** is a cross-sectional view of the unit pixel section **10** taken

along line A-A' in Figure 6A. The image sensor includes a plurality of unit pixel sections 10.

Referring to Figures 6A and 6B, each unit pixel section 10 includes a light receiving diode 11 for performing photo-electric conversion of light incident thereon to generate charges in an amount corresponding to the amount of incident light, and a MOS transistor 12 for detecting a signal corresponding to the amount of incident light. The MOS transistor 12 is adjacent to the light receiving diode 11.

The light receiving diode 11 includes an N-type well region 14 formed in a surface region of a P-type substrate 13, and a P-type well region 15 formed on the N-type well region 14. An area of the P-type well region 15, which is in the light receiving diode 11, acts as a light receiving region and generates charges (holes) when irradiated with light. The P-type well region 15 connects the light receiving diode 11 and the MOS transistor 12 to each other.

The MOS transistor 12 includes an annular gate electrode 16, an N-type source region 17 surrounded by

the gate electrode 16, an N-type drain region 18 provided outside the gate electrode 16, an N-type layer 19 acting as a transistor channel region, and a P-type carrier pocket region 20 acting as a charge accumulation region. The P-type carrier pocket region 20 is a p-type hole pocket region in this example.

The gate electrode 16 is provided so as to surround the source region 17. The source region 17 is provided inside the gate electrode 16. The drain region 18 is provided so as to surround the annular gate electrode 16.

The N-type layer 19 is provided right below the gate electrode 16 as a transistor channel region between the source region 17 and the drain region 18.

The carrier pocket region 20 is provided at a position which is in the P-type well region 15, below the gate electrode 16 and the N-type layer 19, and in the vicinity of the source region 17. Horizontally seen (Figure 6A), the carrier pocket 20 is annular and surrounds the source region 17. Charges generated in the light receiving diode 11 are accumulated in the carrier pocket region 20 through the P-type well region 15. For a signal

read operation, a prescribed unit pixel section **10** is selected by a gate voltage applied to the gate electrode **16**, and an output signal (imaging signal) representing a voltage value corresponding to the amount of the charges accumulated in the carrier pocket region **20** is output from the source region **17**. For a reset operation, the charges accumulated in the carrier pocket region **20** are discharged toward the substrate **13** from the carrier pocket region **20** through the drain region **18** by a gate voltage applied to the gate electrode **16**.

The MOS image sensor includes a plurality of unit pixel sections **10** in a matrix, i.e., in rows and columns. Gate voltages of a selected row and gate voltages of an unselected row are separately controlled by a gate driving circuit (not shown), so that image signals for respective selected unit pixel sections **10** are sequentially read through a selected column.

The operation of the MOS image sensor will be described with reference to Figures **7** and **8**.

Figure **7** shows a potential distribution of the unit pixel section **10** shown in Figures **6A** and **6B** in operation

(during an imaging cycle). In Figure 7, the horizontal axis represents the depth of the MOS image sensor from the surface of a cross-section taken along line B-B' in Figure 6B. In accordance with the depth, the MOS image sensor includes the gate electrode 16, the N-type layer 19 as the channel region, the carrier pocket region 20, the N-type well region 14, and the substrate 13. The vertical axis represents the potential in each of the regions of the MOS image sensor during operations in the imaging cycle. One imaging cycle includes a charge accumulation operation, a signal read operation and a reset operation.

As shown in Figure 7, for the charge accumulation operation, the potential of the gate electrode 16 (gate voltage) is set to V_0, and the charges (holes) are transferred from the light receiving diode 11 to the carrier pocket region 20 and accumulated. The concentration profile of each region is set such that the potential barrier $\Delta\phi_{INJ}$ related to the transfer of the holes from the substrate 13 to the carrier pocket region 20 has a magnitude such that charges are not injected from the substrate 13 into the carrier pocket region 20.

Next, for the signal read operation, the potential of the gate electrode **16** is set to V_1, and the potential of the drain voltage region **18** is set to V_D. Thus, the potential of the N-type layer **19** as the channel region changes in accordance with the amount of the accumulated charges in the carrier pocket region **20**. (For example, the potential of the N-type layer **19** becomes ϕ_0 when the amount of the accumulated charges is 0, and the potential of the N-type layer **19** becomes ϕ_1 when the amount of the accumulated charges is Qs). Such a change in the potential of the N-type layer **19** is read from the source region **17** as an output signal (hereinafter, referred to as an "S signal") corresponding to the amount of the accumulated charges in the unit pixel section **10**.

When the signal read operation is terminated, the potential of the gate electrode **16** is set to V_2, which is high. This starts the reset operation of discharging the charges accumulated in the carrier pocket region **20** toward the substrate **13**. After the reset operation, the potential of the gate electrode **16** is again set to V_1, and a pixel reference signal (hereinafter, referred to as an "N signal") is read from the source electrode **17** in a reset state. After the N signal is read, the operation of the

MOS image sensor is returned to the charge accumulation operation (the potential of the gate electrode **16** is set to V_0). Then, the next imaging cycle is performed. The imaging cycle is repeated in this manner.

Figures **8A** and **8B** are timing diagrams illustrating the gate voltage of each operation (charge accumulation operation, signal read operation, and reset operation) during the imaging cycle. Figure **8A** shows a change in the gate voltage of a selected row, and Figure **8B** shows a change in the gate voltage of an unselected row.

The gate voltage of a selected row changes as shown in Figure **8A**. During the charge accumulation operation, the gate voltage is V_0. The gate voltage is changed to V_1 in period T1, and the S signal is read.

In period T2, the gate voltage is changed to V_2, which is high, and the reset operation is performed. In period T3, the gate voltage is returned to V_1, and the N signal is read. Such a series of operations are performed in each imaging cycle.

In an unselected row (Figure **8B**), the gate voltage

is V_0, and charges are accumulated in the carrier pocket region **20**.

The above-described threshold voltage modulation system MOS image sensor has a problem in that when a potential barrier $\Delta\phi_{RST}$ related to the transfer of the charges (holes) from the carrier pocket region **20** to the substrate **13** exists during the reset operation, the charges partially remain in the carrier pocket region **20** (the amount of the remaining charges is represented by ΔQ).

Figure **7** shows gate voltage V_2 during the reset operation and gate voltage V_2' which is lower than V_2. As represented by the comparison of these two voltages, the potential barrier $\Delta\phi_{RST}$ and the remaining charge amount ΔQ rely on the gate voltage. A value of each of the potential barrier $\Delta\phi_{RST}$ and the remaining charge amount ΔQ decreases as the gate voltage increases and approaches the high voltage V_2.

When the remaining charge amount ΔQ increases due to the existence of the potential barrier $\Delta\phi_{RST}$ increases the level of afterimage in an image. Figure **9** shows the relationship between the remaining charge amount ΔQ and

the level of afterimage.

As shown in Figure 9, the remaining charge amount ΔQ in the carrier pocket region 20 is 0 when the gate voltage is V_{20} or higher. Therefore, the level of afterimage increases as the gate voltage decreases from V_{20}, but no afterimage is generated when the gate voltage is V_{20} or higher.

It is experientially or experimentally known in the field of threshold voltage modulation type MOS image sensors that sensitivity variance (PRNU) among a plurality of unit pixel sections 10 increases when the remaining charge amount ΔQ decreases.

As shown in Figure 9, when the gate voltage V_2 during the reset operation becomes V_{21} (lower than V_{20} at or higher than which no afterimage is generated) or higher, the sensitivity variance (PRNU) rapidly increases.

SUMMARY OF THE INVENTION

According to one aspect of the invention, a solid-state imaging device includes at least one pixel

section; and a control section for controlling an operation of the at least one pixel section. The at least one pixel section includes a light receiving section for outputting charges by performing photo-electric conversion of light incident thereon, and a transistor section having a charge accumulation region for accumulating the charges output by the light receiving section. The transistor section outputs an output signal representing a voltage value corresponding to an amount of charges accumulated in the charge accumulation region. The control section, for resetting the charges accumulated in the charge accumulation region after the output signal is output from the transistor section, injects charges into the charge accumulation region before discharging the accumulated charges from the charge accumulation region.

In one embodiment of the invention, the solid-state imaging device further includes a substrate. The transistor section further includes a gate electrode, a source electrode, and a drain electrode. The control section injects the charges into the charge accumulation region from the substrate by applying a first gate voltage to the gate electrode.

In one embodiment of the invention, the control section discharges the accumulated charges from the charge accumulation region by applying a second gate voltage to the gate electrode. The second gate voltage has a value which causes a prescribed amount of charges to remain in the charge accumulation region.

In one embodiment of the invention, the control section accumulates the charges output from the light receiving section in the charge accumulation region by applying a third gate voltage to the gate electrode.

In one embodiment of the invention, the control section outputs the output signal from the transistor section by applying a fourth gate voltage to the gate electrode.

In one embodiment of the invention, a value of a potential barrier between the substrate and the charge accumulation region when the first gate voltage is applied to the gate electrode is smaller than a value of the potential barrier between the substrate and the charge accumulation region when the third gate voltage is applied to the gate electrode.

In one embodiment of the invention, a value of the second gate voltage is obtained by shifting a gate voltage value necessary to completely discharge the charges accumulated in the charge accumulation region in a direction causing the prescribed amount of charges to remain in the charge accumulation region.

In one embodiment of the invention, the solid-state imaging device includes a plurality of pixel sections which are arranged in a matrix.

In one embodiment of the invention, the solid-state imaging device includes a plurality of pixel sections. The control section applies the third gate voltage to a gate electrode included in at least one unselected pixel section among the plurality of pixel sections. A value of the third gate voltage prevents charges from being injected from the substrate into the charge accumulation region.

In one embodiment of the invention, the at least one pixel section further includes a substrate including a well region. The transistor section includes an annular

gate electrode, a source electrode surrounded by the gate electrode, a drain electrode surrounding the gate electrode, and a channel region provided at a position which is in the well region and below the gate electrode. The charge accumulation region is provided at a position which is in the well region and below the channel region, so as to surround the source electrode. The transistor section is connected to the light receiving section via the well region.

According to another aspect of the invention, a method for driving a solid-state imaging device is provided. The solid-state imaging device includes at least one pixel section; and a control section for controlling an operation of the at least one pixel section. The at least one pixel section includes a light receiving section for outputting charges by performing photo-electric conversion of light incident thereon, and a transistor section having a charge accumulation region for accumulating the charges output by the light receiving section. The method includes the steps of outputting an output signal from the transistor section, the output signal representing a voltage value corresponding to an amount of charges accumulated in the charge accumulation region, and for resetting the charges

accumulated in the charge accumulation region after the output signal is output from the transistor section, injecting charges into the charge accumulation region before discharging the accumulated charges from the charge accumulation region.

In one embodiment of the invention, the at least one pixel includes a substrate, and the transistor section further includes a gate electrode, a source electrode, and a drain electrode. The step of injecting includes the step of injecting charges from the substrate into the charge accumulation region by applying a first gate voltage to the gate electrode.

In one embodiment of the invention, the method further includes the step of discharging the accumulated charges from the charge accumulation region by applying a second gate voltage to the gate electrode. The second gate voltage has a value which causes a prescribed amount of charges to remain in the charge accumulation region.

In one embodiment of the invention, the method further includes the step of accumulating the charges output from the light receiving section in the charge

accumulation region by applying a third gate voltage to the gate electrode.

In one embodiment of the invention, the step of outputting the output signal includes the step of applying a fourth gate voltage to the gate electrode.

The present invention provides the following functions due to the above-described structure.

According to the present invention, for resetting the charges accumulated in the charge accumulation region after the output signal is output from the transistor section, charges are injected into the charge accumulation region before the accumulated charges are discharged from the charge accumulation region. Then, the charges are discharged toward the substrate in the state where a prescribed amount of charges remain in the charge accumulation region. Therefore, a constant amount of charges remain in the charge accumulation region regardless of the amount of charges accumulated during the charge accumulation period (i.e., regardless of the amount of incident light). Thus, no afterimage is generated. Since a constant amount of charges remain in

the charge accumulation region, the sensitivity variance (PRNU) can be kept at a low, stable level.

Since the control section controls voltages in the transistor section, such as the gate voltage, it becomes easy to control the charge injection operation from the substrate into the charge accumulation region and the discharge operation with a constant, small amount of charges remaining in the charge accumulation region. The control section controls the gate voltages of a selected row and the gate voltages of an unselected row separately. Thus, it is made possible to sequentially perform the charge injection operation and the discharge operation for each selected row.

Thus, the invention described herein makes possible the advantages of providing a solid-state imaging device and a method for driving the same for providing a high quality image by suppressing generation of an afterimage in an image and suppressing sensitivity variance among pixel sections.

These and other advantages of the present invention will become apparent to those skilled in the

art upon reading and understanding the following detailed description with reference to the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure **1A** is a block diagram of a solid-state imaging device according to one example of the present invention;

Figure **1B** is a cross-sectional view of a unit pixel section included in the solid-state imaging device shown in Figure **1A**;

Figures **2A** and **2B** show a potential distribution of the unit pixel section included in the solid-state imaging device shown in Figure **1A**;

Figures **3A** and **3B** are timing diagrams illustrating the gate voltage in the solid-state imaging device shown in Figure **1A**;

Figure **4** shows the relationship between the amount of charges remaining in the carrier pocket region and the level of afterimage, and the relationship between the

amount of charges and the sensitivity variance, of the solid-state imaging device **1** shown in Figure **1A**;

Figure **5** is a block diagram illustrating the solid-state imaging device **1** shown in Figure **1A** in more detail;

Figure **6A** is a block diagram illustrating a solid-state imaging device;

Figure **6B** is a cross-sectional view of the solid-state imaging device shown in Figure **6A**;

Figure **7** shows a potential distribution of the unit pixel section shown in Figure **6A**;

Figures **8A** and **8B** are timing diagrams illustrating the gate voltage in the solid-state imaging device shown in Figure **6A**;

Figure **9** shows the relationship between the amount of charges remaining in the carrier pocket region and the level of afterimage, and the relationship between the amount of charges and the sensitivity variance, of the

solid-state imaging device shown in Figure 6A; and

Figures 10A and 10B are timing diagrams illustrating the gate voltage in the solid-state imaging device shown in Figure 1A when applied to a shutter operation.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, the present invention will be described by way of illustrative examples with reference to the accompanying drawings.

Figure 1A is a block diagram illustrating a part of a solid-state imaging device 1 according to one example of the present invention. In this example, the solid-state imaging device 1 is a threshold voltage modulation system MOS image sensor.

The solid-state imaging device 1 includes at least one unit pixel section 10 and a driving control section 2 for controlling the operations of the unit pixel section 10. The unit pixel section 10 includes a substrate 13, a light receiving diode 11 for performing photo-electric

conversion of light incident thereon to generate charges in an amount corresponding to the amount of incident light, and a MOS transistor 12. The MOS transistor 12 includes a carrier pocket region 20 acting as a charge accumulation region for accumulating charges output from the light receiving diode 11. The MOS transistor 12 outputs an output signal (imaging signal) representing a voltage value corresponding to the amount of charges accumulated in the carrier pocket region 20. The driving control section 2, for resetting the charges accumulated in the charge accumulation region 20 after the output signal is output from the MOS transistor 12, injects charges into the carrier pocket region 20 before discharging the charges accumulated in the carrier pocket region 20. The carrier pocket region 20 is a P-type hole pocket region in this example.

The solid-state imaging device 1 shown in Figure 1A includes a plurality of unit pixel sections 10. The plurality of unit pixel sections 10 are provided, for example, in a matrix. The driving control section 2 separately controls the control voltages of the unit pixel section 10 of a selected row and the control voltages of the unit pixel section 10 of an unselected row. The control

voltages are a gate voltage, a source voltage and a drain voltage described below. Thus, the driving control section **2** sequentially reads imaging signals from the unit pixel sections **10** of the selected row through a selected column.

Figure **1A** shows only one unit pixel section **10** for the sake of simplicity but the solid-state imaging device **1** includes the number of unit pixel sections **10** corresponding to the number of pixels. Figure **1B** is a cross-sectional view of the unit pixel section **10** taken along line **a-a'** in Figure **1A**. In Figures **1A** and **1B**, identical elements previously discussed with respect to Figures **6A** and **6B** bear identical reference numerals thereto and the detailed descriptions thereof will be omitted.

As described above, the unit pixel section **10** includes the light receiving diode **11** acting as a light receiving section and a MOS transistor **12** acting as a transistor section for detecting a signal corresponding to the amount of the incident light. The MOS transistor **12** is provided adjacent to the light receiving diode **11**.

The light receiving diode **11** includes an N-type

well region 14 formed in a surface region of a P-type substrate 13, and a P-type well region 15 formed on the N-type well region 14. An area of the P-type well region 15, which is in the light receiving diode 11, acts as a light receiving region and generates charges (holes) corresponding to the amount of light incident thereon.

The MOS transistor 12 includes an annular gate electrode 16, an N-type source region 17 surrounded by the gate electrode 16, an N-type drain region 18 surrounding the gate electrode 16, an N-type layer 19 acting as a transistor channel region provided at a position which is in the P-type well region 15 and right below the gate electrode 16, and a P-type carrier pocket region 20. The P-type carrier pocket region 20 is provided at a position which is in the P-type well region 15, below the gate electrode 16 and the N-type layer 19, and in the vicinity of the source region 17. The carrier pocket region 20 is provided to surround the source region 17 and acts as a charge accumulation region. The MOS transistor 12 is connected to the light receiving diode 11 via the P-type well region 15. The source region 17 acts as a source electrode, and the drain region 18 acts as a drain electrode.

The driving control section 2 controls the voltages of the gate electrode 16, the source electrode 17 and the drain electrode 18 in order to control the charge accumulation operation, the signal read operation, and the reset operation.

For the reset operation, the driving control section 2 applies a gate voltage having a value, capable of injecting charges into the carrier pocket region 20 from the substrate 13, to the gate electrode 16. Then, when discharging the accumulated charges from the carrier pocket region 20 toward the substrate 13, the driving control section 2 applies a gate voltage having a value, capable of causing a prescribed, constant amount of charges to remain in the carrier pocket region 20, to the gate electrode 16. Thus, the sensitivity variance among the plurality of unit pixel sections 10 can be at a low, stable level.

The operation of the solid-state imaging device 1 will be described with reference to Figures 2A, 2B, 3A and 3B.

Figures 2A and 2B show a potential distribution

of the unit pixel section **10** shown in Figures **1A** and **1B** in operation (during an imaging cycle). Figure **2A** shows the potential distribution during the charge accumulation operation and the signal read operation. Figure **2B** shows the potential distribution during the reset operation.

In Figures **2A** and **2B**, the horizontal axis represents the depth of the solid-state imaging device **1** from the surface of a cross-section taken along line **b-b'** in Figure **1B**. In accordance with the depth, the solid-state imaging device **1** includes the gate electrode **16**, the N-type layer **19** as the channel region, the carrier pocket region **20**, the N-type well region **14**, and the substrate **13**. The vertical axis represents the potential in each of the regions of the solid-state imaging device **1** during operations in the imaging cycle.

As shown in Figure **2A**, for the charge accumulation operation, the driving control section **2** sets the potential of the gate electrode **16** to V_M (potential V_M is, for example, equal to potential V_0 in Figure **7**), and the charges (holes) generated in the light receiving diode **11** are transferred to the carrier pocket region **20** and accumulated. The concentration profile of each region is set such that the

potential barrier $\Delta\phi_{INJ}(M)$ between the substrate **13** and the carrier pocket region **20** related to the transfer of the holes from the substrate **13** to the carrier pocket region **20** during the charge accumulation operation (when the gate potential is V_M) has a magnitude such that charges are prevented from being injected from the substrate **13** into the carrier pocket region **20**.

Next, for the signal read operation, the driving control section **2** sets the potential of the gate electrode **16** to V_H (potential V_H is, for example, equal to potential V_1 in Figure 7), and sets the potential of the drain electrode **18** to V_D. Thus, the potential of the N-type layer **19** as the channel region changes in accordance with the amount of the accumulated charges in the carrier pocket region **20**. (For example, the potential of the N-type layer **19** becomes ϕ_0 when the amount of the accumulated charges is 0, and the potential of the N-type layer **19** becomes ϕ_1 when the amount of the accumulated charges is Qs). Such a change in the potential of the N-type layer **19** is read from the source region **17** as an output signal (hereinafter, referred to as an "S signal") corresponding to the amount of the accumulated charges in the unit pixel section **10**.

As shown in Figure 2B, when the signal read operation is terminated, the driving control section 2 sets the potential of the gate electrode 16 to V_L, which is lower than V_M. When the potential of the gate electrode 16 is set to V_L, the value of the potential barrier between the substrate 13 and the carrier pocket region 20 related to the transfer of the holes from the substrate 13 to the carrier pocket region 20 becomes $\Delta\phi_{INJ}(L)$, which is lower than $\Delta\phi_{INJ}(M)$. This causes the holes (i.e., charges) to be injected from the substrate 13 into the carrier pocket region 20. The injected amount of charges at this point is ΔQ_2.

Next, the driving control section 2 sets the potential of the gate electrode 16 to potential V_{21}, which is lower than the potential V_{20} (Figure 4), and discharges the charges accumulated in the carrier pocket region 20 toward the substrate 13. At or higher than V_{20}, no afterimage is generated as described above. The value of the potential V_{21} is obtained by shifting the potential V_{20} required to completely discharge the accumulated charges from the carrier pocket region 20 in a direction causing a prescribed amount of charges to remain in the carrier pocket region 20. The potential barrier $\Delta\phi_{RST}$

between the carrier pocket region **20** and the substrate **13** related to the transfer of the charges (holes) from the carrier pocket region **20** to the substrate **13** is set to a magnitude at which charges in a prescribed charge amount ΔQ_1 are allowed to remain in the carrier pocket region **20** when the potential of the gate electrode **16** is V_{21}. The prescribed charge amount ΔQ_1 is smaller than the injected charge amount ΔQ_2.

After the above-described reset operation, the driving control section **2** again sets the potential of the gate electrode **16** to V_M in the state where the charges remain in the carrier pocket region **20** in an amount of ΔQ_1, and reads the pixel reference signal (hereinafter, referred to as an "N signal") from the source electrode **17**. After the N signal is read, the operation of the MOS image sensor is returned to the charge accumulation operation. Then, the next imaging cycle is performed. The imaging cycle is repeated in this manner.

The concentration profile of each region is set such that the potential barrier $\Delta\phi_{INJ}(L)$ at the gate voltage V_L, the potential barrier $\Delta\phi_{INJ}(M)$ at the gate voltage V_M, and the potential barrier $\Delta\phi_{RST}$ at the gate voltage V_{21}

fulfill the above conditions.

Figures **3A** and **3B** are timing diagrams illustrating the gate voltage of each operation (charge accumulation operation, signal read operation, and reset operation) during the imaging cycle. Figure **3A** shows a change in the gate voltage of a selected row, and Figure **3B** shows a change in the gate voltage of an unselected row. The driving control section **2** sets the voltage of the gate electrode **16** included in at least one unselected pixel section **10** to V_M.

As shown in Figure **3A**, in period T1, the gate voltage is set to V_H, and the S signal is read. Next, in period Tx, the gate voltage is set to V_L, and holes are injected into the carrier pocket region **20** from the substrate **13**. In period T2, the gate voltage is set to V_{21}, and the reset operation for causing the charges in an amount of ΔQ_1 to remain in the carrier pocket region **20** is performed. Then, in period T3, the gate voltage is again set to V_H and the N signal is read. Such a series of operations are repeated for each imaging cycle.

In this example, for the resetting operation,

charges are first injected from the substrate **13** into the carrier pocket region **20**, and then charges are discharged toward the substrate **13** while causing a prescribed constant amount of charges to remain in the carrier pocket region **20**. Therefore, a prescribed constant amount of charges remain in the carrier pocket region **20** regardless of the amount of the charges accumulated during the charge accumulation period (i.e., regardless of the amount of incident light). Therefore, no afterimage is generated. Since a prescribed constant amount of charges remain in the carrier pocket region **20**, the sensitivity variance (PRNU) can be lowered.

Figures **3A** and **3B** show an example of performing a reset operation after the S signal is read. During a shutter operation, only the reset operation is performed without reading any signal. For a reset operation in such a case, charges are injected. Figures **10A** and **10B** are timing diagrams illustrating the gate voltage in the case where the present invention is applied to the shutter operation. Figure **10A** shows a change in the gate voltage of a selected row, and Figure **10B** shows a change in the gate voltage of an unselected row. As shown in Figure **10A**, in a preceding period including period T1, the gate

voltage is set to V_M. Then, the gate is set to V_L in period Tx, and holes are injected into the carrier pocket region **20** from the substrate **13**. Next, the gate voltage is set to V_{21} in period T2, and the reset operation for causing charges in an amount of ΔQ_1 to remain in the carrier pocket region **20** is performed. Then, the gate voltage is set to V_M in a succeeding period including period T3. For performing the shutter operation, the operation shown in Figure **10A** is inserted into the imaging cycle shown in Figure **3A**.

Figure **4** shows the relationship between the amount of charges ΔQ remaining in the carrier pocket region **20** and the level of afterimage, and the relationship between the amount of charges ΔQ and the sensitivity variance (PRNU), of the solid-state imaging device **1** according to the present invention.

As shown in Figure **4**, when the gate voltage during the reset operation is V_{21} or in the vicinity thereof, a constant level of remaining charges ΔQ exist in each of the plurality of unit pixel sections **10**. Therefore, the sensitivity variance (PRNU) can be kept at a low level (low, stable level X) without generating any afterimage.

Therefore, the solid-state imaging device 1 according to the present invention can provide a high quality image.

Figure 5 shows the solid-state imaging device 1 according to the present invention in more detail. In the example shown in Figure 5, the solid-state imaging device 1 includes a 2 pixel × 2 pixel circuit configuration for imaging a two-dimensional image. Figure 5 shows the 2 pixel × 2 pixel circuit configuration for the sake of simplicity, but the present invention is not limited to such a structure. The solid-state imaging device 1 includes the number of unit pixel sections 10 corresponding to the number of pixels.

In the solid-state imaging device 1 shown in Figure 5, a plurality of (four in Figure 5) unit pixel sections 10 are arranged in a matrix, i.e., in rows and columns. In each unit pixel section 10, the gate electrode 12 (G) of the MOS transistor 12 is connected to a gate voltage control section 3 via a gate line 21. The drain electrode 18 (D) (Figure 1B) is connected to a drain voltage control section 4 (drain driving circuit) via a drain line 22. The gate voltage control section 3, the drain voltage control section 4, and a boost section 5 are connected

to a voltage generation section 7 for generating a driving pulse and a driving voltage necessary to realize each of the above-described operations. The source electrode 17 (S) is connected to the boost section 5 (boost circuit) and a horizontal read section 6 (horizontal read circuit) via a source line 23. The horizontal read section 6 is connected to an output circuit 8. The gate voltage control section 3, the drain voltage control section 4, the boost section 5, the voltage generation section 7, the horizontal read section 6, and the output circuit 8 are included in the driving control section 2 (Figure 1). The charge accumulation operation, the signal read operation, and the reset operation are controlled by respective control voltages supplied from the gate voltage control section 3, the drain voltage control section 4, and the boost section 5.

In the solid-state imaging device 1 shown in Figure 5, for selecting an initial gate line 21 by the gate voltage control section 3, gate voltages having a driving waveform shown in Figure 3A (first through fourth gate voltages V_L, V_{21}, V_M and V_H) are applied to the gate line 21 to be selected by the gate voltage control section 3. The other gate lines 21 are placed into an unselected state, and

a gate voltage having a driving waveform shown in Figure 3B (gate voltage V_M) is applied to the unselected gate lines 21 by the gate voltage control section 3.

In the plurality of unit pixel sections 10 which are connected to the selected gate line 21 (unit pixel sections 10 in a selected row), a series of operations of: charge accumulation (third gate voltage V_M) to signal read of the S signal (fourth gate voltage V_H) to hole injection (first gate voltage V_L) to reset with the charges partially remaining (second gate voltage V_{21}) to signal read of the N signal (fourth gate voltage V_H) are sequentially performed. In the plurality of unit pixel sections 10 connected to the unselected gate lines 21 (unit pixel sections 10 in an unselected selected row), the charge accumulation operation (third gate voltage V_M) is performed. The voltage application to the source electrode 17 during the reset operation is performed by the boost section 5 via the source line 23.

The imaging signal (S signal) which is read via the source line 23 during the signal read operation is output to an output terminal via the horizontal read section 6 and the output circuit 8.

In the solid-state imaging device **1** in this example, the gate voltages of a selected row and the gate voltages of an unselected row are separately controlled. This makes it easy to control only the selected row regarding the charge injection from the substrate **13** into the carrier pocket region (charge accumulation region) **20** and the reset operation for causing a constant, small amount of charges to remain in the carrier pocket region **20**. Since a constant amount of charges remain in each carrier pocket region **20**, (i) no afterimage is generated and (ii) the sensitivity variance (PRNU) among the plurality of unit pixel sections **10** can be lowered.

In the solid-state imaging device **1** in this example, the reset operation is performed by injecting charges into only the pixel sections to be reset (which may be all the pixel portions) and then applying a voltage for discharging the charges. Thus, generation of an afterimage and sensitivity variance can be suppressed. Since the charges are injected into target pixel sections during the reset operation, excessive discharging is prevented and thus generation of an afterimage can be prevented. The value of the voltage for discharging the charges may be set to

a level at which the sensitivity variance is low.

The gate voltage changes, for example, as shown in Figures **3A** and **3B**. The source voltage and the drain voltage fundamentally change as in the conventional solid-state imaging device. The source voltage and the drain voltage may be controlled in various manners. For example, Japanese Laid-Open Publication No. 2001-196570 discloses a method for applying a high voltage to the source electrode so as to increase the gate voltage, but many other methods including this method may be used for the present invention.

When the polarity of the elements included in the unit pixel section **10** is inverted, the level relationship of the voltages is also inverted. For example, the polarity of the elements is inverted, the level relationship of V_{21} and V_{20} is inverted from $V_{21} < V_{20}$ to $V_{21} > V_{20}$.

According to the present invention, the reset operation is performed by first injecting charges into the charge accumulation region from the substrate, and then discharging the accumulated charges from the charge

accumulation region toward the substrate while causing a prescribed amount of charges to remain in the charge accumulation region. Therefore, a constant amount of charges remain in the charge accumulation region regardless of the amount of charges accumulated during the charge accumulation period (i.e., regardless of the amount of incident light). Thus, no afterimage is generated. Since a constant amount of charges remain in the charge accumulation region, the sensitivity variance (PRNU) can be kept at a low, stable level. Therefore, the solid-state imaging device according to the present invention provides a high quality image.

Various other modifications will be apparent to and can be readily made by those skilled in the art without departing from the scope and spirit of this invention. Accordingly, it is not intended that the scope of the claims appended hereto be limited to the description as set forth herein, but rather that the claims be broadly construed.